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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/610,753	07/06/2000	Shunpel Yamazaki	SEL 195	5666

7590 01/20/2004

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/610,753	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,21,23,25,27 and 53* is/are pending in the application.

4a) Of the above claim(s) *2,4-20,22,24,26 and 28-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,21,23,25,27 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's arguments, see pages 3 – 4 of the after final amendment, filed December 18, 2003, with respect to the claims have been fully considered and are persuasive. The previous rejections of the claims have been withdrawn, and new rejections are made.

Drawings

2. The corrected drawings were received on December 18, 2003. These drawings are accepted.

Election/Restrictions

3. Claims 2, 4 – 20, 22, 24, 26 and 28 – 52 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (USPAT 5767930) in view of Shimone (JPPAT 6258659) and Adan et al. (USPAT 5841170, Adan).

With regard to claim 1, Kobayashi discloses in figure 1f and column 6, line 66 – column 7, line 29 a semiconductor device. Kobayashi discloses in figure 1f a pixel TFT (10) disposed in a pixel section over a substrate (1), and a driver circuit comprising a p-channel TFT (30) and an n-channel TFT (20), over the substrate. Kobayashi discloses in column 6, line 66 – column 7, line 29 wherein the LCD device has pixel electrodes and interconnection lines. A device such as Kobayashi's with pixel electrodes and interconnection lines needs insulation to work properly. Kobayashi is silent to first and second interlayer insulating films. with a second interlayer insulating film (29) over a gate electrode (27) of the pixel TFT. Shimone discloses in figure 3d a first interlayer insulating film (113) comprising an inorganic insulating material over a gate electrode (106) of a pixel TFT. Shimone discloses in figure 3d a second interlayer insulating film (104) comprising an organic insulating material over the first interlayer insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic insulating film of Shimone in the device of Kobayashi in order to use an insulating material capable of photo imaging as the interlayer dielectric in a working LCD device. Kobayashi discloses in column 7, lines 4 – 14 and the abstract a pixel electrode electrically connected with the pixel TFT. Kobayashi is silent to a pixel electrode having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the second interlayer insulating film. Shimone further teaches a pixel electrode (106) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the first and second interlayer insulating films. Therefore it would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the opening

and pixel electrode of Shimone in the device of Kobayashi in order to use a working configuration of a pixel electrode. Kobayashi discloses in figure 1f wherein the p-channel TFT (30) of the driver circuit comprises a channel forming region (directly below gate (34) and to the left of s/d region (37)) a source region (right 37) and a drain region (left 37, i.e. the s/d region not labeled) in contact with the channel forming region the p-channel TFT of the driver circuit does not have a LDD region. Kobayashi discloses in figure 1f wherein the n-channel TFT (20) of the driver circuit comprises a channel forming region (region between (29)), an n-type impurity region of a first concentration (29) which forms at least one LDD region in contact with the channel forming region, and a source region and a drain region (26) in contact with the at least one LDD region. Kobayashi and Shimone not disclose that the LDD region is partly overlapping a gate electrode (26). Adan teaches in figure 29; column 2, lines 17 – 25; column 11, lines 58 – 60; column 12, lines 9 – 11; and column 13, lines 49 – 51 wherein an n-channel TFT (61a) of the driver circuit comprises a channel forming region (65), an n-type impurity region of a first concentration which forms at least one LDD region (71) in contact with the channel forming region and partly overlapping a gate electrode (66), and a source region (63) and a drain region (64) in contact with the at least one LDD region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Kobayashi and Shimone in order to increase the breakdown voltage of the transistor as stated by Adan in column 2, lines 17 – 25. Kobayashi discloses in figure 1f wherein the pixel TFT (10) comprises a channel forming region (between 19), at least one LDD region (19) in contact with the channel forming region, and a source region (left 16) and a drain region (right (16) in contact with the at least one LDD region.

With regard to claim 25, the semiconductor device of Kobayashi, Adan, and Shimone could obviously be part of a personal computer.

6. Claims 3, 21, 23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Shimone, Hioki (JPPAT 8234212) and Adan.

With regard to claim 3, Kobayashi discloses in figure 1f a semiconductor device. Kobayashi discloses in figure 1f a pixel TFT (10) disposed in a pixel section over a first substrate (1). Kobayashi discloses in figure 1f a driver circuit comprising a p-channel TFT (30) and an n-channel TFT (20), over the first substrate. Kobayashi discloses in column 6, line 66 – column 7, line 29 wherein the LCD device has pixel electrodes and interconnection lines. A device such as Kobayashi's with pixel electrodes and interconnection lines needs insulation to work properly. Kobayashi is silent to first and second interlayer insulating films. with a second interlayer insulating film (29) over a gate electrode (27) of the pixel TFT. Shimone discloses in figure 3d a first interlayer insulating film (113) comprising an inorganic insulating material over a gate electrode (106) of a pixel TFT. Shimone discloses in figure 3d a second interlayer insulating film (104) comprising an organic insulating material over the first interlayer insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic insulating film of Shimone in the device of Kobayashi in order to use an insulating material capable of photo imaging as the interlayer dielectric in a working LCD device. Kobayashi discloses in column 7, lines 4 – 14 and the abstract a pixel electrode electrically connected with the pixel TFT. Kobayashi is silent to a pixel electrode having a light reflective surface over the second interlayer insulating film, and is

electrically connected with the pixel TFT through an opening in the second interlayer insulating film. Shimone further teaches a pixel electrode (106) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the first and second interlayer insulating films. Therefore it would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the opening and pixel electrode of Shimone in the device of Kobayashi in order to use a working configuration of a pixel electrode. Kobayashi discloses in column 6, line 66 – column 7, line 29 a liquid crystal sandwiched between the first and a transparent second substrate. Kobayashi and Shimone do not disclose a columnar spacer. Hioki discloses in figure 1 at least a columnar spacer (24) covering an opening. Hioki discloses in figure 1 a second substrate (26) having a transparent conductive film stuck to a first substrate (14) through the at least one columnar spacer. Hioki discloses in figure 1 a liquid crystal (13) sandwiched between the first and second substrates. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the columnar spacer of Hioki in the device of Kobayashi and Shimone in order to create a liquid crystal display with constant distance between substrates thus improving device performance. Kobayashi discloses in figure 1f wherein the p-channel TFT (30) of the driver circuit comprises a channel forming region (directly below gate (34) and to the left of s/d region (37)) a source region (right 37) and a drain region (left 37, i.e. the s/d region not labeled) in contact with the channel forming region the p-channel TFT of the driver circuit does not have a LDD region. Kobayashi discloses in figure 1f wherein the n-channel TFT (20) of the driver circuit comprises a channel forming region (region between (29)), an n-type impurity region of a first concentration (29) which forms at least one LDD region in contact with the channel forming

region, and a source region and a drain region (26) in contact with the at least one LDD region. Kobayashi, Shimone, and Hioki not disclose that the LDD region is partly overlapping a gate electrode (26). Adan teaches in figure 29; column 2, lines 17 – 25; column 11, lines 58 – 60; column 12, lines 9 – 11; and column 13, lines 49 – 51 wherein an n-channel TFT (61a) of the driver circuit comprises a channel forming region (65), an n-type impurity region of a first concentration which forms at least one LDD region (71) in contact with the channel forming region and partly overlapping a gate electrode (66), and a source region (63) and a drain region (64) in contact with the at least one LDD region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Kobayashi, Shimone, and Hioki in order to increase the breakdown voltage of the transistor as stated by Adan in column 2, lines 17 – 25. Kobayashi discloses in figure 1f wherein the pixel TFT (10) comprises a channel forming region (between 19), at least one LDD region (19) in contact with the channel forming region, and a source region (left 16) and a drain region (right (16) in contact with the at least one LDD region.

With regard to claim 21, Hioki discloses in figure 1 a columnar spacer (24) formed over TFTs (22) of the driver circuit.

With regard to claim 23, Hioki discloses in figure 1 a columnar spacer formed to cover source wirings of TFTs.

With regard to claim 27, the semiconductor device of Kobayashi, Shimone, Hioki, and Adan could obviously be part of a personal computer.

7. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Shimone, Takasu (USPAT 5982002, Takasu), Adan, and Matsumoto (USPAT 5323042).

With regard to claim 53, Kobayashi discloses in figure 1f a semiconductor device. Kobayashi discloses in figure 1f a pixel TFT (10) disposed in a pixel section over a first substrate (1). Kobayashi discloses in figure 1f a driver circuit comprising a p-channel TFT (30) and an n-channel TFT (20), over the first substrate. Kobayashi discloses in column 6, line 66 – column 7, line 29 wherein the LCD device has pixel electrodes and interconnection lines. A device such as Kobayashi's with pixel electrodes and interconnection lines needs insulation to work properly. Kobayashi is silent to first and second interlayer insulating films. with a second interlayer insulating film (29) over a gate electrode (27) of the pixel TFT. Shimone discloses in figure 3d a first interlayer insulating film (113) comprising an inorganic insulating material over a gate electrode (106) of a pixel TFT. Shimone discloses in figure 3d a second interlayer insulating film (104) comprising an organic insulating material over the first interlayer insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic insulating film of Shimone in the device of Kobayashi in order to use an insulating material capable of photo imaging as the interlayer dielectric in a working LCD device. Kobayashi discloses in column 7, lines 4 – 14 and the abstract a pixel electrode electrically connected with the pixel TFT. Kobayashi is silent to a pixel electrode having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the second interlayer insulating film. Shimone further teaches a pixel electrode (106) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an

opening in the first and second interlayer insulating films. Therefore it would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the opening and pixel electrode of Shimone in the device of Kobayashi in order to use a working configuration of a pixel electrode. Kobayashi discloses in column 7, lines 4 – 14 source wirings over the second interlayer insulating film. Kobayashi and Shimone are silent to a source wiring over the second interlayer insulating film. Kobayashi and Shimone also do not teach an alignment film and liquid crystal over the pixel electrode and the source wiring. Takasu teaches in figure 1 an alignment film (114) over a pixel electrode (112) and a source wiring (111). Takasu teaches in figure 1 a liquid crystal sandwiched between the alignment film and an opposed substrate (115). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the source wiring, alignment film and liquid crystal of Takasu in the device of Kobayashi and Shimone for aligning the orientation of liquid crystal molecules as stated by Takasu in column 7, lines 28 – 33. Kobayashi discloses in figure 1f wherein the p-channel TFT (30) of the driver circuit comprises a channel forming region (directly below gate (34) and to the left of s/d region (37)) a source region (right 37) and a drain region (left 37, i.e. the s/d region not labeled) in contact with the channel forming region the p-channel TFT of the driver circuit does not have a LDD region. Kobayashi discloses in figure 1f wherein the n-channel TFT (20) of the driver circuit comprises a channel forming region (region between (29)), an n-type impurity region of a first concentration (29) which forms at least one LDD region in contact with the channel forming region, and a source region and a drain region (26) in contact with the at least one LDD region. Kobayashi, Shimone, and Hioki not disclose that the LDD region is partly overlapping a gate electrode (26). Adan teaches in figure 29;

column 2, lines 17 – 25; column 11, lines 58 – 60; column 12, lines 9 – 11; and column 13, lines 49 – 51 wherein an n-channel TFT (61a) of the driver circuit comprises a channel forming region (65), an n-type impurity region of a first concentration which forms at least one LDD region (71) in contact with the channel forming region and partly overlapping a gate electrode (66), and a source region (63) and a drain region (64) in contact with the at least one LDD region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Kobayashi, Shimone, and Hioki in order to increase the breakdown voltage of the transistor as stated by Adan in column 2, lines 17 – 25. Kobayashi discloses in figure 1f wherein the pixel TFT (10) comprises a channel forming region (between 19), at least one LDD region (19) in contact with the channel forming region, and a source region (left 16) and a drain region (right (16) in contact with the at least one LDD region. Kobayashi, Shimone, Takasu, and Adan do not teach that the pixel electrode and the source wiring are formed simultaneously. Matsumoto discloses in figure 1 wherein the pixel electrode and the source wiring are formed, simultaneously. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the simultaneous forming of the pixel electrode and source wiring of Matsumoto in the device of Kobayashi, Shimone, Takasu, and Adan in order to minimize production steps, thus increasing productivity and reducing process costs. It should be noted that the limitation "wherein the pixel electrode and the source wiring are formed, simultaneously" is a product by process limitation which bears no patentable weight in a device claim.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 3, 21, 23, 25, 27, and 53 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703) 308-6236. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
January 13, 2004

Tom Thomas